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Docket No.: M4065.0477/P477  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Kevin M. Devereaux

3 / 4 formal Drawings  
E. Ullio  
12-3-01

Application No.: 09/939,636

Group Art Unit: N/A

Filed: August 28, 2001

Examiner: Not Yet Assigned

For: METHOD AND APPARATUS FOR WAFER  
LEVEL TESTING OF SEMICONDUCTOR  
USING SACRIFICIAL ON DIE POWER  
AND GROUND METALIZATION

SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents  
Washington, DC 20231

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Dear Sir:

Submitted herewith is one set (five sheets, Figures 1-5) of formal drawings for filing in the above-identified Patent application. Kindly substitute the enclosed formal drawings for the informal drawings submitted with the originally filed application.

Dated: November 20, 2001

Respectfully submitted,

By 

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